Optical Bus for a Multi-Core Processor

DeepTech

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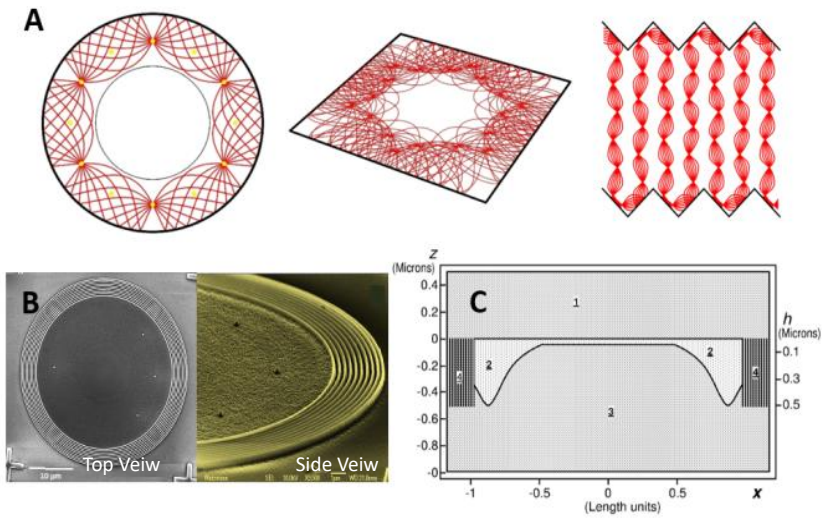
A compact on-chip optical layer that replaces traditional wiring in multi-core processors using silicon photonics.
This innovative approach significantly reduces power consumption, heat generation, and space requirements, enabling higher core densities and improved inter-core communication.



(A) Top-view schematics of various optical bus geometries. (B) SEM images of a prototype fabricated via e-beam lithography. (C) Cross-sectional schematic of the optical bus: (1) and (3) cladding layers; (2) light-guiding layer; (4) Bragg mirror. Light propagation is controlled by the thickness-dependent refractive index of the silicon layer.

APPLICATIONS

- High-performance computing and information processing, including AI, data centers, and consumer electronics
- Optical interconnects for deep learning, robotics, neuromorphic hardware, and signal processing
- Scalable communication platforms for telecom and next-gen computing platforms

DEVELOPMENT STAGE

Miniature prototypes have been fabricated and successfully tested, demonstrating the feasibility of the technology. In order to achieve the full potential of the technology, prototypes need to be connected externally to many lasers and detectors

ADVANTAGES

Direct and wireless inter-core communication, with scalable connectivity (up to 1000-fold increase)

Increased computing power, reduced power consumption and heat output

Waveguide fabrication is compatible with traditional CMOS fabrication technologies

Point-to-point communication without crosstalk