CNT-Based Structure for High-Resolution Semiconductor Process Control

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Overview

With the continuous trend of electronic component miniaturization, process control technologies must keep up with component size reduction. Defects that were so far negligible, are now posing critical operation obstacles, and are more difficult to identify as scales are reduced to <10 nm. This new technology developed by a group of researchers from the Weizmann Institute of Science is a carbon nanotube (CNT)-based single-electron transistor (SET), enabling noninvasive, simultaneous visualization of currents and potentials of flowing electrons at the single-electron level. In addition, it can be used to detect defects in buried structures, a key challenge in semiconductor process control. This state-of-the-art noninvasive instrument exhibits sensitivity up to X1000 higher than that of characterization technologies currently in use. This technology can serve as a valuable tool for the semiconductor manufacturing industry, ensuring retention of both yield and high quality standard production.

The Need

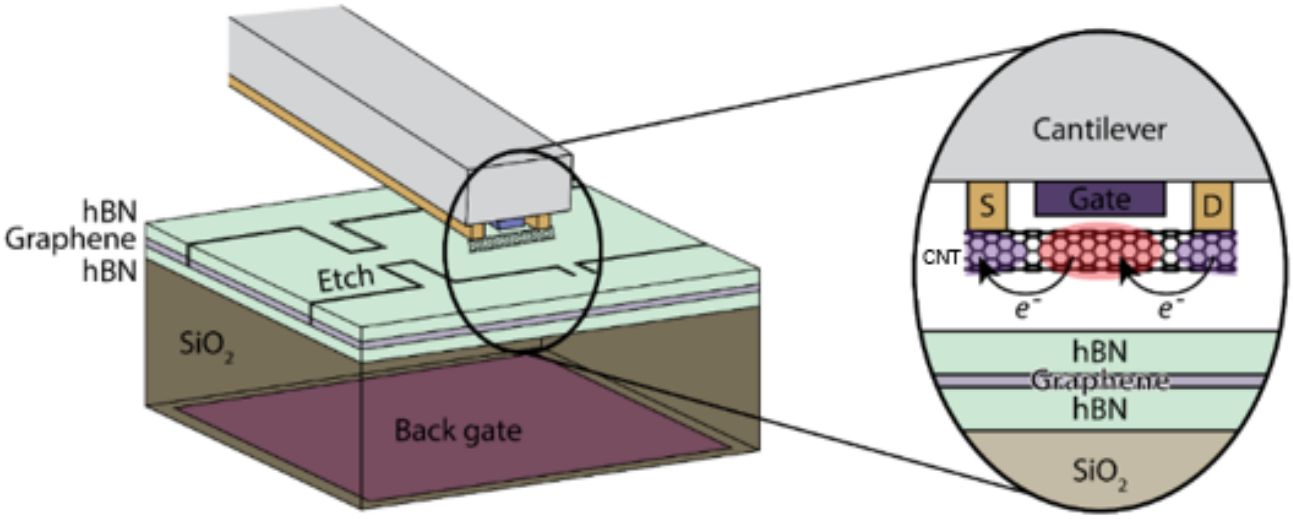
The rapid advancements in electronics, including the ongoing miniaturization and increased structure complexity, require the development of supporting analysis techniques for failure detection to ensure device operation quality. Of particular importance is the measurement of currents and potentials transferred through small structures and the detection of failure spots, particularly in buried structures. Among the most prevalent potential measurement methods are the Kelvin probe, which although has the advantage of being a non-contact device has a relatively low sensitivity, and the scanning tunneling microscope-based potentiometer that has higher sensitivity, yet requires the tunneling of electrons from the device under study and thus cannot be employed as a non-contact inspection method. Common devices for the detection of currents, such as the scanning SQUID and the Hall probe, suffer from relatively low measurement accuracy. No instrument enables the simultaneous detection of both currents and potentials.

The Solution

The proposed technology is based on a single-electron transistor (SET) made of carbon nanotubes (CNTs) which enables simultaneous visualization of both the currents and potentials of flowing electrons, eliminating the need to use several different instruments. It uses a non-contact approach that can accurately map information in buried structures even below an insulating layer, with sensitivity reaching three orders of magnitude higher than that of existing techniques. Its features render it suitable for high-sensitivity defect analysis in the microelectronic fabrication industry.

Technology Essence

The method takes advantage of the high voltage sensitivity of the scanning SET. It operates by applying a small AC bias voltage across a device of interest. The SET is used to isolate and image the potentials of the flowing electrons induced by the bias voltage. This can be done with a voltage imaging sensitivity of ~2uV/sqrt(Hz), three orders of magnitude (x1000) higher than that of the Kelvin probe technology, and can thus accurately map the potentials of flowing electrons. The current imaging sensitivity is ~10nA/um/sqrt(Hz) for semiconductors, which is X100 higher than that of SQUID-like techniques or scanning NV centers. As no charge is directly transferred between the SET and the device under study (unlike tunneling-based techniques), this method is ideally suited for high-sensitivity imaging potentials of flowing electrons in buried structures, which are increasingly prevalent. By applying a weak magnetic field perpendicular to the plane of the device, the SET can be used to map the local Hall voltage produced by flowing electrons, enabling imaging of the local current density. Unlike existing approaches, this method requires only local voltage measurements (instead of the global magnetic field), and is therefore less prone to artifacts. Imaging both the potential and current of flowing electrons relies on local voltage measurements, and can therefore be performed simultaneously, instead of requiring two separate apparatus/imaging tools.



A schematic presentation of the arrangement of the carbon nanotube on the SET detection arm. The nanotube is connected to source and drain electrodes (yellow) and suspended above multiple gates (blue). The CNT structure is designed to scan the device of interest with no charge directly transferred between the probe and the inspected area.

Applications and Advantages

Advantages

- Simultaneous imaging of potentials and current flow
- Non-invasive and no-contact method
- Up to x1000 higher sensitivity, both on the surface and in buried structures, even below an insulating layer
- Does not entail global measurement of magnetic field
- Detects changes at the single-electron level

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Applications

- Advanced non-contact inspection method for the semiconductor production line
- CNT-based nanoscale transistor
- AFM-like inspection tool with high sensitivity for multiple applications

Development Status

The group of researchers has demonstrated the validity of the invention on several graphene-based nanoscale devices (published in: *Nature Nanotechnology*, **volume 14**, 480â€“487 (2019) [1]). A series of experiments is planned to fully demonstrate the utility of the invention. A patent was granted for this invention and an additional patent application is pending.

Market Opportunity

According to a KPMG report from the â€œGlobal Semiconductor Industry Outlook 2019â€, due to new developments, semiconductor production is becoming increasingly costly and â€œIncreasing R&D costsâ€ was flagged as the biggest issue facing the industry. The ongoing changes in the semiconductor fabrication industry require new, advanced inspection technologies that will keep up with the advancements in production technologies, reduce defect rates and maintain high yield. According to a recent report, the semiconductor inspection equipment market is estimated at $3.6 billion and is anticipated to increase at an 8.7% CAGR during 2019-2028. This evaluation is higher than the evaluated market increase in the broader semiconductor market, with a 6.9% CAGR during 2019-2024. This difference between expected market value of the inspection equipment and the broader semiconductor market further emphasizes the need for the development of novel production technologies and supporting defect analysis technologies. The value proposition of a novel, non-contact and high-resolution defect analysis technology, enabling maintained high production quality and yield in complex and reduced size chip structures is therefore obvious.

Patent Status

USA Granted: 10,069,094